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Menu

- What is I²C and TWI?
- TWI Data Transfer
- TWI Registers

See docs/examples on web-site:
doc8331, do2585, doc2564

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What is I²C and TWI?

- Inter-Integrated Circuit (I²C, I2C, or IIC)
  >Established by Phillips
- Two Wire Interface (TWI)
  >Synonymous with I²C
  >Implemented on various systems including ATMEL
- TWI is meant to be more flexible then SPI
- Asynchronous serial data transmission in half duplex mode
  >Data transfer flows in one direction at a time
  >Data transfer is on a bidirectional, open-drain bus
- A Master controls the process, while one or more Slaves respond to the queries of the Master

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What is I²C and TWI?

- A unique address is given to each slave device connected to the bus
  - >7-bit address
  - >Master uses this to address a slave and initiate data transaction
- Multiple masters may be connected to the same bus (multi-master environment)
  - >Only one master may own the bus at a given time
  - >Devices may act as either slave or master
- TWI on XMEGA may operate in both Master and Slave mode
  - >Mode of operation chosen by TWI Status Register and TWI Control Register

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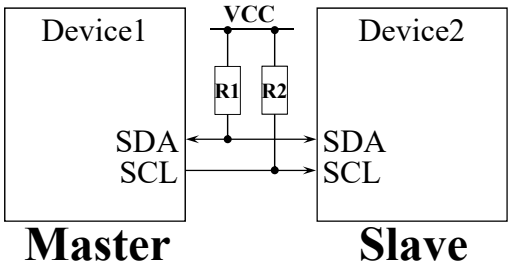
Simple TWI Setup

- 2 Interface Signals
  - >**SCL** – **S**erial **CL**ock
  - >**SDA** – **S**erial **DA**ta
- Pull up resistors are used on both lines
  - >Devices pull down
  - >Resistors pull up



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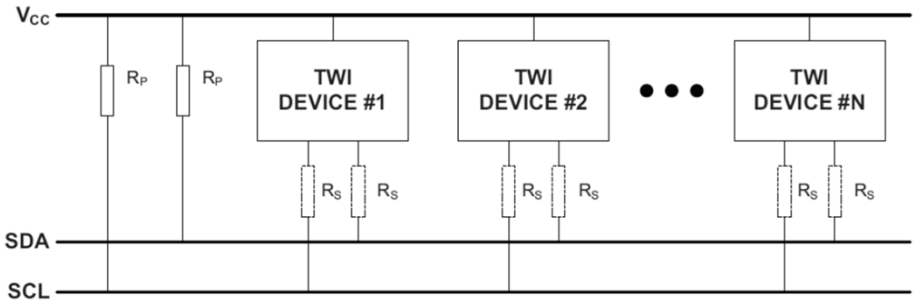
doc8331: Figure 21-1

XMEGA TWI

- SDA and SCL are open collector (Wired-AND) lines
- Pull-up resistors provide a high level on the lines when no connected devices are driving the bus
- On XMEGA, PORTS C, D, E, and F.



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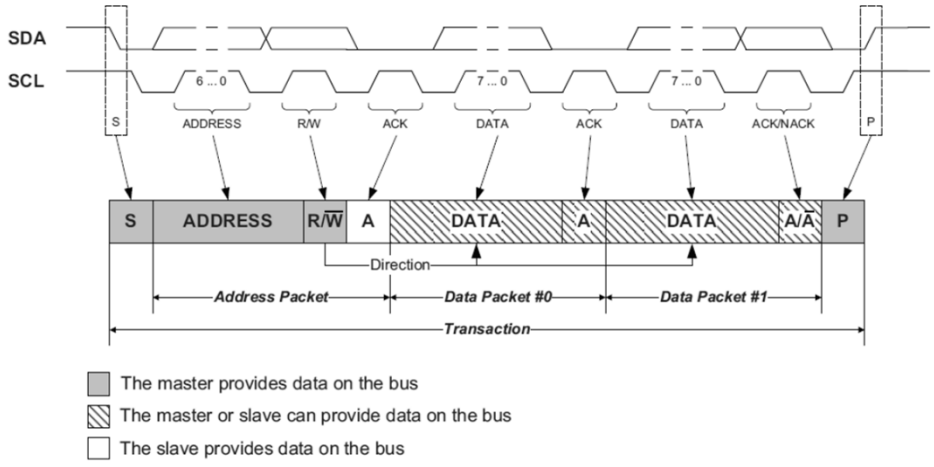
doc8331: Figure 21-2

TWI Data Transfer Sequence

- Master indicates data transfer by issuing START condition (**S**)



doc8331: Figure 21-2

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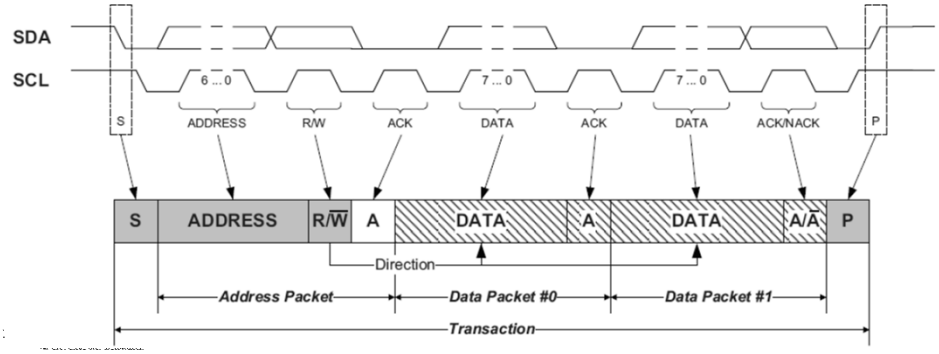
TWI Data Transfer Sequence

The master provides data on the bus
The master or slave can provide data on the bus
The slave provides data on the bus

- Master then sends slave address (**ADDRESS**) [7 bits] and whether the data transfer is a read or write data (**R/~W**)
- Slave should Acknowledge (**A**) or **not**-Acknowledge (**~A**)



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doc8331: Figure 21-2

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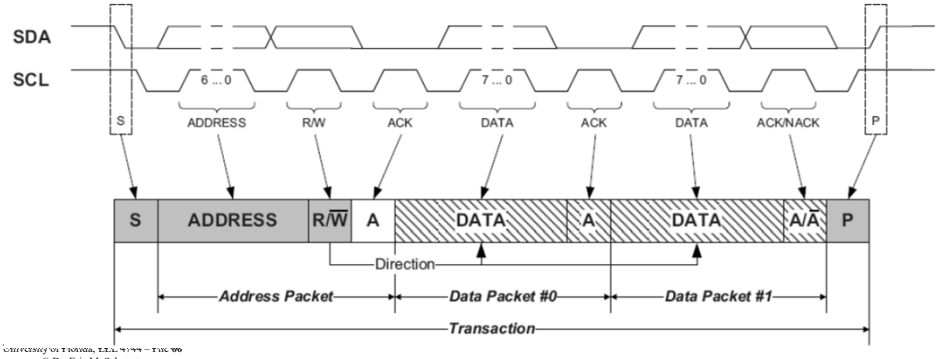
TWI Data Transfer Sequence

The master provides data on the bus
The master or slave can provide data on the bus
The slave provides data on the bus

- Master or Slave place 1 or more **DATA** packets on the bus
  > Receiver Acknowledges or not-Acknowledges after each packet
- Master issues a **STOP** condition (**P**)



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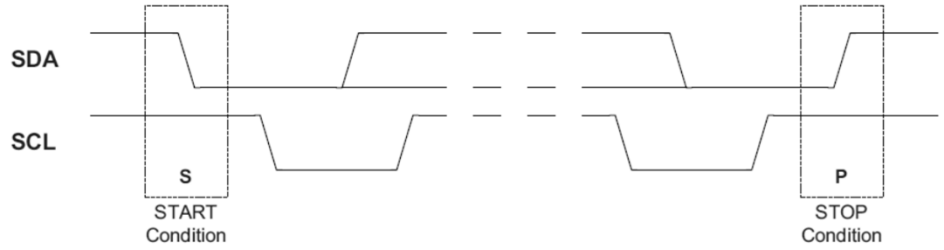
TWI Data Transfer Start and Stop

- Start condition is signaled by indicating a falling edge for **SDA** while **SCL** is kept high
- Stop condition is signaled by indicating a rising edge for **SDA** while **SCL** is kept high
- Between Start and Stop, no other masters should attempt to initiate a transfer



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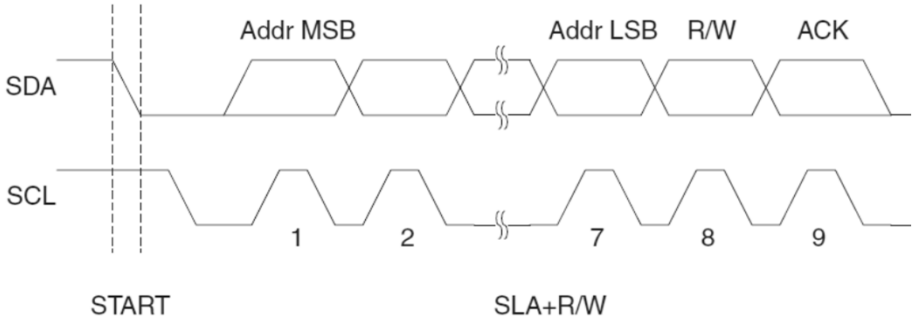
TWI Data Transfer Address Packet

- One Address packet follows the **START** bit
- Address Packet consists of 9 bits
  - > 7-bit Address (MSB first) from master
  - > 1 read/write control bit from master
  - > 1 acknowledge bit from slave



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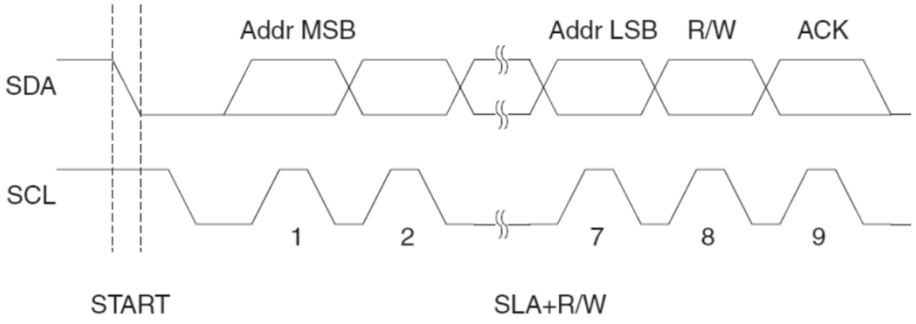
TWI Data Transfer Address Packet

- Read/Write bit
  > Low indicates a Master write
  > High indicates a Master read
- Slave recognizing their address will send the acknowledge
  > All other slaves will keep bus lines released until next **START** bit



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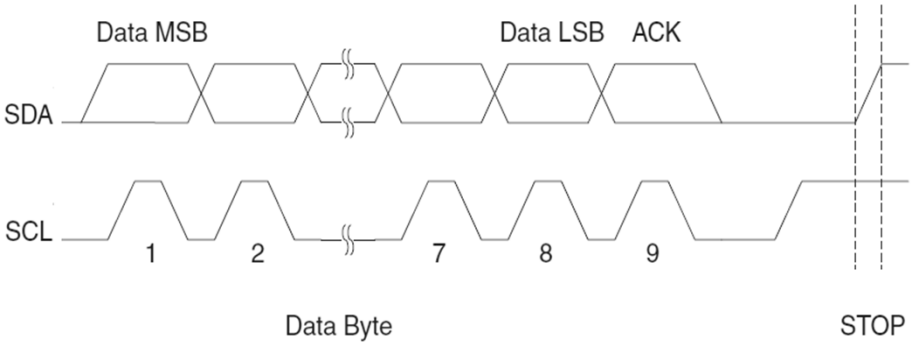
TWI Data Transfer Data Packet

- One or more Data packets follow the acknowledge of the address packet
- Data Packet consists of 9 bits
  > 8-bit Data (MSB first) from slave or master
  > 1 acknowledge bit from receiver (slave or master)



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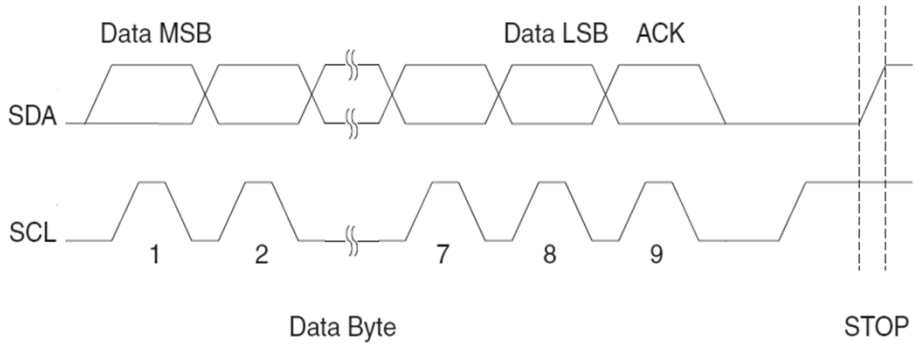
TWI Data Transfer Data Packet

- During the transfer, the Master generates the SCL



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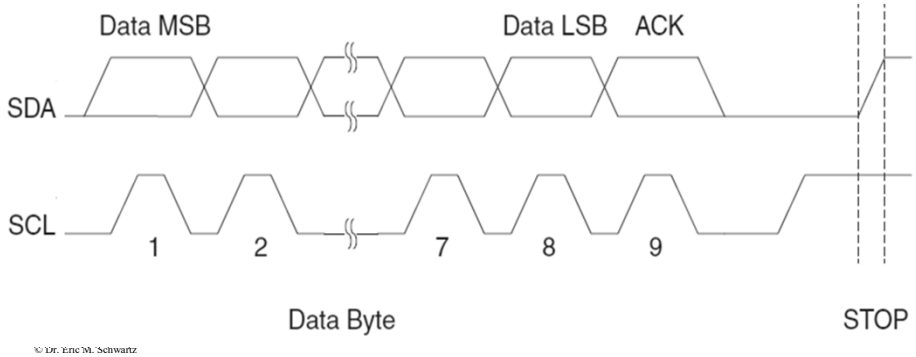
TWI Data Transfer Bit Transfers

- SDA values can only be changed during low period of SCL
- Address and Data packets are transferred in 8-bit packets followed by a single-bit non-Acknowledge or Acknowledge
  - > **Acknowledge** - The addressed device pulls SDA line down in the 9th SCL cycle
  - > **Non-Acknowledge** - The addressed device leaves the SDA line high in the 9th SCL cycle



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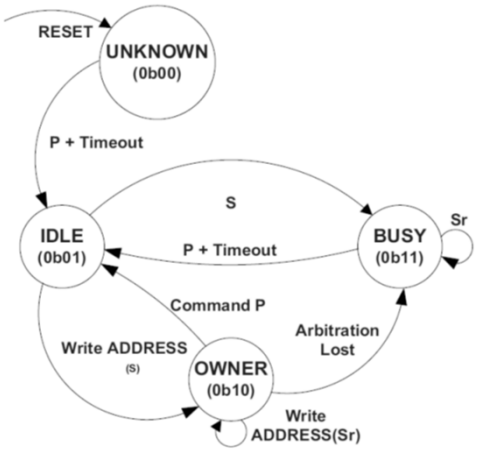
TWI Data Transfer State Diagram



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TWI Data Transfer Interrupts

- While TWINT Flag is set, SCL is held low
  - > This allows software to complete tasks before the next TWI transmission is allowed to continue
- The TWI Status Register will detail which event caused the interrupt
- TWINT is set in the following cases:
  - > START/REPEATED START condition is sent
  - > SLA+RW is sent
  - > ADDRESS Byte is sent
  - > Arbitration is lost
  - > TWI is addressed by slave address or a general call
  - > A DATA Byte is received
  - > STOP or REPEATED START is received while being addressed as a slave
  - > Bus error occurred due to an illegal START or STOP condition

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XMEGA
TWI Registers

- TWIx_CTRL

- TWIx_MASTER_CTRLA
- TWIx_MASTER_CTRLB
- TWIx_MASTER_CTRLC
- TWIx_MASTER_STATUS
- TWIx_MASTER_BAUD
- TWIx_MASTER_ADDR
- TWIx_MASTER_DATA

- TWIx_SLAVE_CTRLA
- TWIx_SLAVE_CTRLB
- TWIx_SLAVE_STATUS
- TWIx_SLAVE_ADDR
- TWIx_SLAVE_DATA
- TWIx_SLAVE_ADDRMASK

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XMEGA TWI MASTER
CTRL & CTRLA Register

- CTRL – SDA Hold Time, External Driver Interface Enable

	7	6	5	4	3	2	1	0	
+0x00	-	-	-	-	-	SDAHOLD1	SDAHOLD0	EDIEN	**CTRL**
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- CTRLA – Interrupt Level, Read Interrupt Enable, Write Interrupt Enable, Enable TWI Master

	7	6	5	4	3	2	1	0	
+0x00	INTLVL1	INTLVL0	RIEN	WIEN	ENABLE	-	-	-	**CTRLA**
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

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XMEGA TWI MASTER
CTRLB & CTRLC Register

- CTRLB – Inactive Bus Timeout, Quick Command Enable, Smart Mode Enable

	7	6	5	4	3	2	1	0	
+0x01	-	-	-	-	TIMEOUT1	TIMEOUT0	QCEN	SMEN	**CTRLB**
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- CTRLC – Acknowledge Action, Command

	7	6	5	4	3	2	1	0	
+0x02	-	-	-	-	-	ACKACT	CMD1	CMD0	**CTRLC**
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

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XMEGA TWI MASTER
STATUS & BAUD Register

- STATUS – Read and Write Interrupt Flag, Clock Hold, Received Acknowledge, Arbitration Level, Bus Error, Bus State

	7	6	5	4	3	2	1	0	
+0x03	RIF	WIF	CLKHOLD	RXACK	ARBLOST	BUSERR	BUSSTATE1	BUSSTATE0	**STATUS**
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- BAUD – Calculated Baud Rate

	7	6	5	4	3	2	1	0	
+0x04	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0	**BAUD**
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

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XMEGA TWI MASTER
Baud Rate Calculation

- Frequency relation between system clock and TWI bus clock

$$f_{twi} = \frac{f_{sys}}{2(5 + (BAUD))} Hz$$

- Baud rate may be set to a value resulting in a TWI bus clock frequency (f_{twi}) equal or less than 100kHz or 400kHz

$$\text{BAUD} = \frac{f_{sys}}{2f_{twi}} - 5$$

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XMEGA TWI MASTER
ADDR & DATA Register

• ADDR – Address Register

	7	6	5	4	3	2	1	0	
+0x05	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	**ADDR**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

• DATA – Data Register

	7	6	5	4	3	2	1	0	
+0x06	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	**DATA**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

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XMEGA TWI SLAVE
CTRLA & CTRLB Register

- CTRLA – Interrupt Level, Data Interrupt Enable, Address/Stop Interrupt Enable, Enable TWI Master, Stop Interrupt Enable, Promiscuous Mode Enable, Smart Mode Enable

	7	6	5	4	3	2	1	0	
+0x00	INTLVL1	INTLVL0	DIEN	APIEN	ENABLE	PIEN	PMEN	SMEN	**CTRLA**
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- CTRLB – Acknowledge Action, Command

	7	6	5	4	3	2	1	0	
+0x01	-	-	-	-	-	ACKACT	CMD1	CMD0	**CTRLB**
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

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XMEGA TWI SLAVE
STATUS & ADDR Register

- STATUS – Data Interrupt Flag, Address/Stop Interrupt Flag, Clock Hold, Received Acknowledge, Collision, TWI Slave Bus Error, Read/Write Direction, Slave Address or Stop

	7	6	5	4	3	2	1	0	
+0x02	DIF	APIF	CLKHOLD	RXACK	COLL	BUSERR	DIR	AP	**STATUS**
Read/Write	R/W	R/W	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- ADDR – Address Register

	7	6	5	4	3	2	1	0	
+0x03	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	**ADDR**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

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XMEGA TWI SLAVE DATA & ADDRMASK Register

• DATA – Data Register

	7	6	5	4	3	2	1	0	
+0x04	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	**DATA**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

• ADDRMASK – Address Mask, Address Enable

	7	6	5	4	3	2	1	0	
+0x05	ADDRMASK7	ADDRMASK6	ADDRMASK5	ADDRMASK4	ADDRMASK3	ADDRMASK2	ADDRMASK1	ADDREN	**ADDR**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

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The End!